PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-204524

(43)Date of publication of application : 30.07.1999

(51)Int.Cl. H01L 21/3205

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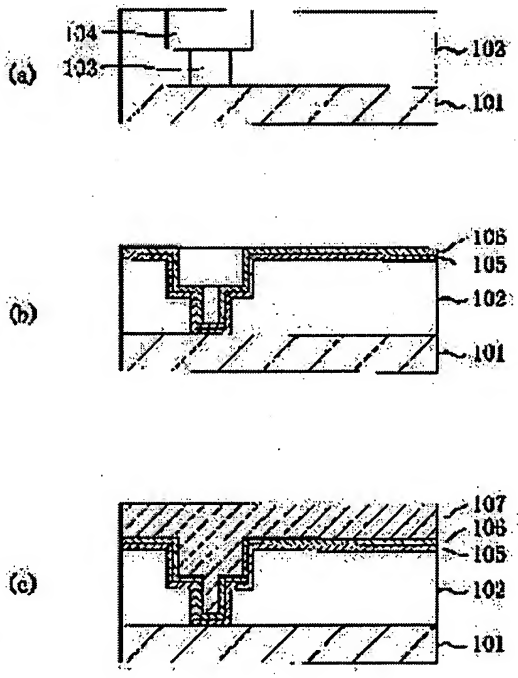
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE OF THE SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a high semiconductor device with high reliability having embedded wiring in which conductivity and electromigration resistance is satisfactory.

SOLUTION: A contact hole 103 and a recessed groove 104 for wiring are formed on an interlayer insulating film 102 accumulated on a semiconductor substrate 101, and then a TiN/Ti film 105 which is a diffusion preventing film is formed on the wall face of the contact hole 103 and the recessed groove 104 for wiring. A copper alloy film 106, in which Ag is included in Cu is accumulated on the TiN/Ti film 105 through sputtering method, and a copper film 107 is accumulated on the copper alloy film 106 by a CVD method or a plating method. Then, Ag included in the copper alloy film 106 is diffused to the copper film 107 by heat treatment, so that the copper alloy film in which Erg is included in Cu can be formed. Then, the contact and the embedded wiring constituted of the copper alloy, in which Ag is included in Cu can be simultaneously formed by operating a CMP method to the copper alloy film.



LEGAL STATUS

[Date of request for examination] 13.01.1998

[Date of sending the examiner's decision of

rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number] 3040745

[Date of registration] 03.03.2000

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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CLAIMS

[Claim(s)]
[Claim 1] It is the semiconductor device characterized by consisting of a copper alloy with which it is the semiconductor device which has embedding wiring, and Ag, Nb, or aluminum 2O3 contained said embedding wiring in Cu.
[Claim 2] Said copper alloy is a semiconductor device according to claim 1 characterized by 1 or less % of the weight of Ag coming to contain in Cu.
[Claim 3] Said copper alloy is a semiconductor device characterized by 0.4 or less % of the weight of Nb coming to contain in Cu.
[Claim 4] It is the semiconductor device which it is the semiconductor device which has the insulator layer formed after embedding wiring and this embedding wiring, and said insulator layer contains aluminum 2O3, and is characterized by said embedding wiring consisting of a copper alloy which said aluminum 2O3 comes to spread in Cu.
[Claim 5] The crevice formation process which forms the crevice for wiring in the interlayer insulation film deposited on the semi-conductor substrate, The 1st metal membrane formation process which forms the 1st metal membrane which becomes the wall surface of said crevice for wiring from the 1st metal which Ag, Nb, or aluminum 2O3 contained in Cu, The 2nd metal membrane formation process which forms the 2nd metal membrane which consists of the 2nd metal which uses Cu or Cu as a principal component on said 1st metal membrane so that said crevice for wiring may be embedded, By making said 2nd metal membrane diffuse Ag, Nb, or aluminum 2O3 which heat-treats to said semi-conductor substrate, and is contained in said 1st metal membrane The manufacture approach of the semiconductor device characterized by having the embedding wiring formation process which is set to Cu from the copper alloy which Ag, Nb, or aluminum 2O3 contained, and which embeds and forms wiring.
[Claim 6] Said 1st metal membrane formation process includes the process which covers the whole surface and deposits said 1st metal membrane on said interlayer insulation film including said crevice for wiring. Said 2nd metal membrane formation process Said embedding wiring formation process is the manufacture approach of the semiconductor device according to claim 5 characterized by including the process which removes said the 1st metal membrane and 2nd metal membrane which have been exposed on said interlayer insulation film including the process which covers the whole surface and deposits said 2nd metal membrane on said 1st metal membrane.
[Claim 7] Said 2nd metal membrane formation process is the manufacture approach of the semiconductor device according to claim 5 characterized by including the process which deposits said 2nd metal membrane with a CVD method or plating including the process on which said 1st metal membrane formation process deposits said 1st metal membrane by the spatter.
[Claim 8] The crevice formation process which forms the crevice for wiring in the interlayer insulation film deposited on the semi-conductor substrate, The 1st metal membrane formation process which continues and forms in the whole surface the 1st metal membrane which consists of the 1st metal which uses Cu or Cu as a principal component on said interlayer insulation film including said crevice for wiring so that said crevice for wiring may be embedded, The 2nd metal membrane formation process

which forms the 2nd metal membrane which consists of the 2nd metal containing Ag, Nb, or aluminum 2O3 on said 1st metal membrane, The diffusion process which makes said 1st metal membrane diffuse Ag, Nb, or aluminum 2O3 which heat-treats to said semi-conductor substrate, and is contained in said 2nd metal membrane, The manufacture approach of the semiconductor device characterized by having removed said the 1st metal membrane and 2nd metal membrane which have been exposed on said interlayer insulation film, and having the embedding wiring formation process which consists of a copper alloy which Ag, Nb, or aluminum 2O3 contained in Cu, and which embeds and forms wiring.
[Claim 9] The crevice formation process which forms the crevice for wiring in the interlayer insulation film deposited on the semi-conductor substrate, The 1st metal membrane formation process which forms the 1st metal membrane which becomes said crevice for wiring from the 1st metal which uses Cu or Cu as a principal component so that the space section may remain on this 1st metal membrane, The 2nd metal membrane formation process which forms the 2nd metal membrane which consists of the 2nd metal which Ag, Nb, or aluminum 2O3 contained on said 1st metal membrane so that said space section may be embedded and it may not expose on said interlayer insulation film, By making said 1st metal membrane diffuse Ag, Nb, or aluminum 2O3 which heat-treats to said semi-conductor substrate, and is contained in said 2nd metal membrane The manufacture approach of the semiconductor device characterized by having the embedding wiring formation process which is set to Cu from the copper alloy which Ag, Nb, or aluminum 2O3 contained, and which embeds and forms wiring.
[Claim 10] The crevice formation process which forms the crevice for wiring in the interlayer insulation film deposited on the semi-conductor substrate, The 1st metal membrane formation process which forms the 1st metal membrane which becomes said crevice for wiring from the 1st metal which uses Cu or Cu as a principal component so that said crevice for wiring may be embedded and it may not expose on said interlayer insulation film, The 2nd metal membrane formation process which forms the 2nd metal membrane which consists of the 2nd metal containing Ag, Nb, or aluminum 2O3 on said 1st metal membrane, By making said 1st metal membrane diffuse Ag, Nb, or aluminum 2O3 which heat-treats to said semi-conductor substrate, and is contained in said 2nd metal membrane The manufacture approach of the semiconductor device characterized by having the embedding wiring formation process which is set to Cu from the copper alloy which Ag, Nb, or aluminum 2O3 contained, and which embeds and forms wiring.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which has embedding wiring, and its manufacture approach.
[0002]
[Description of the Prior Art] In LSI formed on the silicon substrate after 0.18-micrometer generation, since it is impossible to disregard delay by CR component of wiring to improvement in the speed of a transistor, it is desirable to use a conductive high metal, i.e., the small metal of specific resistance, as a wiring material. then, aluminum wiring (3micro ohm-cm of specific resistance) -- replacing with -- more -- low -- the examination using Cu wiring [****] (1.7micro ohm-cm of specific resistance) is progressing.
[0003] Moreover, since the consistency of the flowing current is increasing metal wiring for every generation with detailed-izing of the component which constitutes LSI, the metal atom which constitutes metal wiring at the time of current impression needs to be pushed on an electron, needs to move, and it is necessary to raise the resistance also to the phenomenon of the electromigration which metal wiring disconnects. It is expected that it will be expected that deformation, i.e., migration of an atom, cannot take place easily since the melting point is high compared with aluminum, and electromigration resistance of Cu will also be high.
[0004]
[Problem(s) to be Solved by the Invention] However, although metal wiring which consists of Cu is extremely excellent about conductivity, if wiring width of face becomes more detailed, it will be considered that a problem remains in respect of electromigration resistance. For example, it is reported by detailed metal wiring about 0.3-micrometer width of face that electromigration resistance gets worse [Y.Igarashi et al, VLSI Symp., p.76, and 1996]. Therefore, raising electromigration resistance by alloying is examined like the case of aluminum wiring.
[0005] Then, the Cu-Mg alloy [T.Tatewaki et al, IEDM., p.293, and 1995], the Cu-Zr alloy [Y.Igarashi et al, VLSI Symp., p.76, and 1996], the Cu-Sn alloy, etc. are proposed as a wiring material.
[0006] However, although wiring which consists of copper alloys, such as a Cu-Mg alloy, a Cu-Zr alloy, or a Cu-Sn alloy, is excellent in respect of electromigration resistance, a problem remains in respect of conductivity.
[0007] In view of the above, this invention aims at offering the semiconductor device excellent in conductivity and electromigration resistance with the high dependability which embeds and has wiring by offering the wiring material which can aim at coexistence with improvement in conductivity, and improvement in electromigration resistance.
[0008]
[Means for Solving the Problem] The ingredient of tension strength with a large invention-in-this-application person thought that it should excel also in electromigration resistance. As a result which the copper atom which constitutes copper alloy wiring moves, when a current is passed to copper alloy

wiring, while compressive stress increases, tensile stress occurs in the part to which copper atoms decreased in number, and copper alloy wiring disconnects the reason in the part to which copper atoms decreased in number by the part which the copper atom increased. Therefore, the copper alloy with large tension strength must be excellent in electromigration resistance. Then, when the copper alloy which reached in tension strength and was excellent in both conductivity was used as a wiring material, the conclusion that copper alloy wiring with the high dependability excellent in conductivity and electromigration resistance should be obtained was reached.

[0009] When searched for the copper alloy which reached in tension strength among various kinds of copper alloys, and was excellent in both conductivity, the data (wait ****, p.692, 1997 besides Sakai) shown in drawing 8 were found out. According to the property Fig. shown in drawing 8 , the Cu-Nb alloy, the Cu-Ag alloy, and 2OCu-aluminum3 alloy found out that it was the copper alloy which reached in tension strength among various kinds of copper alloys, and was excellent in both conductivity. In addition, in drawing 8 , %IACS shows the rate of conductivity to the conductivity of a pure copper.

[0010] If it embeds using the copper alloy with which Nb, Ag, or aluminum 2O3 was contained in Cu and wiring is formed so that the above examination may show, a semiconductor device with the high dependability excellent in conductivity and electromigration resistance will be obtained.

[0011] Embedding wiring is Ag, Nb, or aluminum 2O3 to Cu for the semiconductor device with which the 1st semiconductor device concerning this invention has embedding wiring. It consists of a contained copper alloy.

[0012] According to the 1st semiconductor device, embedding wiring is set to Cu from the Cu-Nb alloy, the Cu-Ag alloy, or 2OCu-aluminum3 alloy which Ag, Nb, or aluminum 2O3 comes to contain, and as shown in the property Fig. of drawing 8 , these Cu-Nb alloy, a Cu-Ag alloy, and 2OCu-aluminum3 alloy reach in tension strength, and are excellent in both conductivity.

[0013] As for a copper alloy, in the 1st semiconductor device, it is desirable that 1 or less % of the weight of Ag comes to contain in Cu.

[0014] Moreover, as for a copper alloy, in the 1st semiconductor device, it is desirable that 0.4 or less % of the weight of Nb comes to contain in Cu.

[0015] An insulator layer contains aluminum 2O3 for the semiconductor device which has the insulator layer by which the 2nd semiconductor device concerning this invention was formed after embedding wiring and this embedding wiring, and embedding wiring is set to Cu from the copper alloy which aluminum 2O3 comes to spread.

[0016] According to the 2nd semiconductor device, embedding wiring is set to Cu from 2OCu-aluminum3 alloy which aluminum 2O3 comes to contain, and as shown in the property Fig. of drawing 8 , this 2OCu-aluminum3 alloy reaches in tension strength, and is excellent in both conductivity. Moreover, since the insulator layer formed after embedding wiring contains aluminum 2O3, it embeds aluminum 2O3 contained in an insulator layer, and wiring is made to diffuse it, and it can form easily in Cu 2OCu-aluminum3 alloy which aluminum 2O3 comes to contain. In this case, since aluminum 2O3 has insulation, it can also be used as an insulator layer as it is.

[0017] The manufacture approach of the 1st semiconductor device concerning this invention The crevice formation process which forms the crevice for wiring in the interlayer insulation film deposited on the semi-conductor substrate, They are Ag, Nb, or aluminum 2O3 to Cu in the wall surface of the crevice for wiring. The 1st metal membrane formation process which forms the 1st metal membrane which consists of the 1st contained metal, The 2nd metal membrane formation process which forms the 2nd metal membrane which consists of the 2nd metal which uses Cu or Cu as a principal component on the 1st metal membrane so that the crevice for wiring may be embedded, Ag, Nb, or aluminum 2O3 which heat-treats to a semi-conductor substrate and is contained in the 1st metal membrane By diffusing the 2nd metal membrane It has the embedding wiring formation process which is set to Cu from the copper alloy which Ag, Nb, or aluminum 2O3 contained and which embeds and forms wiring.

[0018] According to the manufacture approach of the 1st semiconductor device, at Cu on the wall surface of the crevice for wiring formed in the interlayer insulation film Ag, Nb or aluminum 2O3 After forming the 1st metal membrane which consists of the 1st contained metal, Ag, Nb, or aluminum 2O3

which forms the 2nd metal membrane which consists of the 2nd metal which uses Cu or Cu as a principal component on this 1st metal membrane, performs heat treatment after that, and is contained in the 1st metal membrane Since the 2nd metal membrane is diffused, They are Ag, Nb, or aluminum 2O3 to Cu. It can consist of a contained copper alloy, and can embed, and wiring can be formed.
[0019] Since the metal membrane of the copper system which uses Cu or Cu as a principal component is difficult dry etching, by the way, embedding wiring DAMASHIN which embeds the metal membrane of a copper system in the crevice for wiring since the crevice for wiring is formed in the interlayer insulation film -- according to the manufacture approach of the 1st semiconductor device, although formed of law in many cases it is set to Cu from the copper alloy which Ag, Nb, or aluminum 2O3 contained -- embedding -- wiring -- DAMASHIN -- it can form by law. Moreover, since the contact hole is formed in the crevice bottom for wiring, if a metal membrane is embedded in both a contact hole and the crevice for wiring at coincidence, the contact and embedding wiring which consist of a copper alloy by the dual DAMASHIN method can be formed in coincidence.
[0020] In the manufacture approach of the 1st semiconductor device the 1st metal membrane formation process The process which covers the whole surface and deposits the 1st metal membrane on an interlayer insulation film including the crevice for wiring is included. The 2nd metal membrane formation process It is desirable to include the process which removes the 1st metal membrane and 2nd metal membrane which have exposed the embedding wiring formation process on an interlayer insulation film including the process which covers the whole surface and deposits the 2nd metal membrane on the 1st metal membrane.
[0021] In the manufacture approach of the 1st semiconductor device, it is desirable to include the process on which the 2nd metal membrane formation process deposits the 2nd metal membrane with a CVD method or plating including the process on which the 1st metal membrane formation process deposits the 1st metal membrane by the spatter.
[0022] By the way, in the generation whose design rule is 0.18 micrometers, a contact hole is a diameter of 0.25 micrometer, and it becomes a depth of about 0.8 micrometers, and it is predicted that a depth of about 0.5 micrometers is needed also about the crevice for wiring. If it is going to form such detailed wiring structure using the dual DAMASHIN method, the depth needs to embed a copper alloy by about 1.3 micrometers at the hole (hole whose aspect ratio is about five) whose path is about 0.25 micrometers. However, according to the present technique, in a CVD method and plating, although the metal membrane of a pure copper can be deposited, the metal membrane of a copper alloy cannot be deposited. Moreover, according to the spatter, the metal membrane of a copper alloy can be deposited, but since an overhang will be generated if it is going to deposit on the high crevice for wiring of an aspect ratio, it is difficult [it] to embed a metal membrane by the spatter in the high crevice for wiring which is an aspect ratio.
[0023] However, if the process on which the 2nd metal membrane formation process deposits the 2nd metal membrane with a CVD method or plating is included including the process on which the 1st metal membrane formation process deposits the 1st metal membrane by the spatter After forming the 1st metal membrane which becomes the wall surface of the crevice for wiring from the 1st metal which Ag, Nb, or aluminum 2O3 contained in Cu by the spatter, Since the 2nd metal membrane which consists of the 2nd metal which uses Cu or Cu as a principal component is deposited with a CVD method or plating excellent in step coverage nature, the 1st metal membrane and 2nd metal membrane can be embedded in the crevice for wiring.
[0024] The manufacture approach of the 2nd semiconductor device concerning this invention The crevice formation process which forms the crevice for wiring in the interlayer insulation film deposited on the semi-conductor substrate, The 1st metal membrane formation process which continues and forms in the whole surface the 1st metal membrane which consists of the 1st metal which uses Cu or Cu as a principal component on an interlayer insulation film including the crevice for wiring so that the crevice for wiring may be embedded, They are Ag, Nb, or aluminum 2O3 on the 1st metal membrane. The 2nd metal membrane formation process which forms the 2nd metal membrane which consists of the 2nd metal to contain, Ag, Nb, or aluminum 2O3 which heat-treats to a semi-conductor substrate and is

contained in the 2nd metal membrane The diffusion process which the 1st metal membrane is made to diffuse, The 1st metal membrane and 2nd metal membrane which have been exposed on an interlayer insulation film are removed, and they are Ag, Nb, or aluminum 2O3 to Cu. It has the embedding wiring formation process which consists of a contained copper alloy and which embeds and forms wiring.
[0025] After forming the 1st metal membrane which consists of the 1st metal which uses Cu or Cu as a principal component on an interlayer insulation film including the crevice for wiring formed in the interlayer insulation film according to the manufacture approach of the 2nd semiconductor device, They are Ag, Nb, or aluminum 2O3 on this 1st metal membrane. The 2nd metal membrane which consists of the 2nd metal to contain is formed. Then, Ag, Nb, or aluminum 2O3 which is heat-treated and is contained in the 2nd metal membrane Since the 1st metal membrane is diffused, they are Ag, Nb, or aluminum 2O3 to Cu. It can consist of a contained copper alloy, and can embed, and wiring can be formed.
[0026] After especially the manufacture approach of the 2nd semiconductor device covers the whole surface and forms the 1st metal membrane so that the crevice for wiring may be embedded, in order that it may form the 2nd metal membrane on this 1st metal membrane, the front face of the 2nd metal membrane is almost flat. Therefore, the 2nd Ag, Nb, or aluminum 2O3 from a metal membrane It can be spread more to homogeneity.
[0027] The manufacture approach of the 3rd semiconductor device concerning this invention The crevice formation process which forms the crevice for wiring in the interlayer insulation film deposited on the semi-conductor substrate, The 1st metal membrane formation process which forms the 1st metal membrane which becomes a crevice for wiring from the 1st metal which uses Cu or Cu as a principal component so that the space section may remain on this 1st metal membrane, They are Ag, Nb, or aluminum 2O3 on the 1st metal membrane. The 2nd metal membrane formation process which forms the 2nd metal membrane which consists of the 2nd contained metal so that the space section may be embedded and it may not expose on an interlayer insulation film, Ag, Nb, or aluminum 2O3 which heat-treats to a semi-conductor substrate and is contained in the 2nd metal membrane By diffusing the 1st metal membrane They are Ag, Nb, or aluminum 2O3 to Cu. It has the embedding wiring formation process which consists of a contained copper alloy and which embeds and forms wiring.
[0028] After forming the 1st metal membrane which consists of the 1st metal which uses Cu or Cu as a principal component in the crevice for wiring formed in the interlayer insulation film according to the manufacture approach of the 3rd semiconductor device, They are Ag, Nb, or aluminum 2O3 on this 1st metal membrane. The 2nd metal membrane which consists of the 2nd contained metal is formed. Then, Ag, Nb, or aluminum 2O3 which is heat-treated and is contained in the 2nd metal membrane Since the 1st metal membrane is diffused, they are Ag, Nb, or aluminum 2O3 to Cu. It can consist of a contained copper alloy, and can embed, and wiring can be formed.
[0029] After forming the 1st metal membrane in the crevice for wiring especially according to the manufacture approach of the 3rd semiconductor device so that the space section may remain at this 1st metal membrane top, Since it forms so that the space section may be embedded in the 2nd metal membrane on this 1st metal membrane and it may not expose on an interlayer insulation film, and heat treatment is performed after that, the process which removes the 1st and 2nd metal membranes exposed on the interlayer insulation film becomes unnecessary.
[0030] The manufacture approach of the 4th semiconductor device concerning this invention The crevice formation process which forms the crevice for wiring in the interlayer insulation film deposited on the semi-conductor substrate, The 1st metal membrane formation process which forms the 1st metal membrane which becomes a crevice for wiring from the 1st metal which uses Cu or Cu as a principal component so that the crevice for wiring may be embedded and it may not expose on an interlayer insulation film, They are Ag, Nb, or aluminum 2O3 on the 1st metal membrane. The 2nd metal membrane formation process which forms the 2nd metal membrane which consists of the 2nd metal to contain, Ag, Nb, or aluminum 2O3 which heat-treats to a semi-conductor substrate and is contained in the 2nd metal membrane By diffusing the 1st metal membrane They are Ag, Nb, or aluminum 2O3 to Cu. It has the embedding wiring formation process which consists of a contained copper alloy and which

embeds and forms wiring.
[0031] After forming the 1st metal membrane which consists of the 1st metal which uses Cu or Cu as a principal component in the crevice for wiring formed in the interlayer insulation film according to the manufacture approach of the 4th semiconductor device, They are Ag, Nb, or aluminum 2O3 on this 1st metal membrane. The 2nd metal membrane which consists of the 2nd metal to contain is formed. Then, Ag, Nb, or aluminum 2O3 which is heat-treated and is contained in the 2nd metal membrane Since the 1st metal membrane is diffused, they are Ag, Nb, or aluminum 2O3 to Cu. It can consist of a contained copper alloy, and can embed, and wiring can be formed.
[0032] After forming so that the crevice for wiring may be embedded in the 1st metal membrane in the crevice for wiring and it may not expose on an interlayer insulation film, in order to form the 2nd metal membrane on this 1st metal membrane especially according to the manufacture approach of the 4th semiconductor device, the front face of the 2nd metal membrane is almost flat.
[0033]
[Embodiment of the Invention] (1st operation gestalt) Copper alloy wiring in the semiconductor device concerning the 1st operation gestalt of this invention and its manufacture approach are explained hereafter, referring to drawing 1 (a) - (c) and drawing 2 (a), and (b).
[0034] First, as shown in drawing 1 (a), a contact hole 103 and the concave slot 104 for wiring are formed in the interlayer insulation film 102 deposited on the semi-conductor substrate 101. The path of a contact hole 103 may be about 0.25 micrometers.
[0035] Next, as shown in drawing 1 (b), it continues on the whole surface on the interlayer insulation film 102 including a contact hole 103 and the concave slot 104 for wiring, and the TiN/Ti film 105 which consists of the upper TiN film which prevents the diffusion to lower layer Ti film, the interlayer insulation film 102 of Cu, and the semi-conductor substrate 101 which raise adhesion with the semi-conductor substrate 101 is deposited.
[0036] Next, the copper alloy film 106 which has 40nm thickness is deposited on the TiN/Ti film 105 by the spatter using the target of the copper alloy which consists of Ag Cu-1% of the weight. In this case, since step coverage nature of a spatter generally is not good, the small contact hole 103 of an about 0.25-micrometer diameter and the concave slot 104 for wiring cannot be completely embedded with the copper alloy film 106. The reason is that the copper alloy film 106 will overhang [near the opening of the small contact hole 103 of a path] if the copper alloy film 106 is deposited by the spatter.
[0037] Then, the CVD method or plating which was excellent in step coverage nature after the aforementioned spatter is performed, and as shown in drawing 1 (c), the copper film 107 which has the film 106 (480nm) about 11 times the thickness of a copper alloy is deposited on the copper alloy film 106. Thereby, a contact hole 103 and the concave slot 104 for wiring are completely embedded by the copper alloy film 106 and the copper film 107. the case where electrolytic plating is used as plating in order to raise surface surface smoothness in the CVD method of Cu -- a substrate -- low -- since Cu film [****] is required, in a CVD method or plating, it is required to use the copper alloy film 106 for a substrate.
[0038] Next, by performing heat treatment of about 400 degrees C, and making the Cu film 107 diffuse Ag of the copper alloy film 106, as shown in drawing 2 (a), the copper alloy film 108 which consists of Ag Cu-0.085% of the weight is formed.
[0039] By the way, about the content of Ag in the copper alloy film 108, under the temperature of about 500 degrees C, the solid-solution limit of Ag in Cu is about 1 % of the weight, and when Ag is made to contain more than it, it has a possibility of depositing locally [the phase which uses Ag as a principal component] in the copper alloy film 108. Therefore, considering being 500 degrees C or less, the temperature of heat treatment in a semi-conductor process has 1 or less desirable % of the weight as a content of Ag.
[0040] Next, by performing the CMP method as opposed to the TiN/Ti film 105 and the copper alloy film 108, and removing the TiN/Ti film 105 and the copper alloy film 108 which have been exposed on an interlayer insulation film 102, as shown in drawing 2 (b), the contact 109 and the embedding wiring 110 which consist of copper alloy film 108 are formed. Then, it continues on the embedding wiring 110

and an interlayer insulation film 102 on the whole surface, and the silicon nitride film 111 which prevents the diffusion to the upper part of Cu which constitutes the embedding wiring 110 is deposited.
[0041] The recrystallizing temperature of the copper alloy film 108 which consists of Cu-0.085-% of the weight Ag formed in the 1st operation gestalt is higher than 250 degrees C which is the recrystallizing temperature of a pure copper, and is 400 degrees C (1223 the Japan Institute of Metals besides a ditch, p 1981). Since I hear that it is hard to deform that recrystallizing temperature is high plastically, it is and a hillock and a void cannot produce the copper alloy film 108 easily, it is proved that electromigration resistance improves.
[0042] Moreover, in the copper alloy film 108 which consists of Ag Cu-0.085% of the weight, since the concentration of Ag is about 50 ppm, the conductivity of the copper alloy film 108 is 1.7microohm-cm almost equivalent to a pure copper (J. S.Smart et al., Trans.AIME, 147 (1942), 48). Therefore, the conductivity of the copper alloy film 108 does not fall compared with a pure copper. On the other hand, if it consists of Cu-Zr alloy film already known, it embeds and about 50 ppm of Zr are added in wiring, while electrical conductivity will rise to 2.2microohm-cm, Zr and Cu react, and it is CuZrx. Since there is a problem of being easy to make a compound, the copper alloy film 108 which consists of Cu-Ag is more advantageous like the 1st operation gestalt.
[0043] As explained above, it consists of copper alloy film 108, and embeds, and wiring 110 is excellent in both conductivity and electromigration resistance.
[0044] By the way, with the present technique, while being unable to deposit the copper alloy film which consists of Cu-Ag with a CVD method or plating, the copper alloy film cannot be completely embedded by the spatter in the small contact hole of a path. Then, in the 1st operation gestalt, while depositing thinly the copper alloy film 106 which consists of Ag Cu-1% of the weight by the spatter, after depositing a copper film 107 thickly with a CVD method or plating on the copper alloy film 106, the copper alloy film 108 which consists of Ag Cu-0.085% of the weight is formed by performing heat treatment and making a copper film 107 diffuse Ag of the copper alloy film 106.
[0045] Moreover, since the copper alloy film 106 deposited by the spatter has the property which carries out orientation in a field (111), it carries out orientation of the copper film 107 deposited with a CVD method or plating on the copper alloy film 106 to a field (111) in response to the effect of a substrate. Therefore, field Uchihara child spacing can deposit the copper film 107 almost equal to the field (111) of the copper alloy film 106 with a CVD method or plating. Moreover, since Cu is the same fcc crystal as aluminum, the field which is the maximum **** (111) tends to serve as a cause of an open circuit, but since the field (111) of a copper film 107 is carrying out orientation to parallel with the principal plane of the semi-conductor substrate 11, it embeds, and it is hard coming to disconnect wiring 110, and it also has the advantage which consists of copper alloy film 108 that electromigration resistance improves further.
[0046] In addition, the copper alloy film 106 and copper film 107 which consist of Ag Cu-1% of the weight are made to react nearly completely, and the TiN film of the upper layer which constitutes the TiN/Ti film 105 may be made to contain Ag in the 1st operation gestalt, although the copper alloy film 108 which consists of Ag Cu-0.085% of the weight was formed instead of depositing the copper alloy film 106 which consists of Ag Cu-1% of the weight. In this case, it is desirable on a film deposition process to constitute a copper film 107 from a copper film of the upper layer deposited with lower layer copper film, CVD method, or plating deposited by the spatter.
[0047] Moreover, if the front face of an interlayer insulation film 102 and the semi-conductor substrate 101 is processed with the ammonia plasma etc. and diffusion of Cu is prevented, it is not necessary to deposit diffusion prevention film like the TiN/Ti film 105.
[0048] Moreover, in the 1st operation gestalt, although the Cu-Ag alloy proposed newly was used as copper alloy film 106, when conductivity may become low somewhat, a Cu-Sn alloy, a Cu-Mg alloy, or a Cu-Zr alloy may be used.
[0049] (2nd operation gestalt) Copper alloy wiring in the semiconductor device concerning the 2nd operation gestalt of this invention and its manufacture approach are explained hereafter, referring to drawing 3 (a) - (c) and drawing 4 (a) - (c).

[0050] First, as shown in drawing 3 (a), a contact hole 203 and the concave slot 204 for wiring are formed in the interlayer insulation film 202 deposited on the semi-conductor substrate 201. The path of a contact hole 203 may be about 0.25 micrometers.
[0051] Next, as shown in drawing 3 (b), it continues on the whole surface on the interlayer insulation film 202 including a contact hole 203 and the concave slot 204 for wiring, and the TiN/Ti film 205 which consists of the upper TiN film which prevents the diffusion to lower layer Ti film, the interlayer insulation film 202 of Cu, and the semi-conductor substrate 201 which raise adhesion with the semi-conductor substrate 201 is deposited.
[0052] Next, with a CVD method or plating, after depositing the lower layer copper film 206 on the TiN/Ti film 205 by the spatter using the target which consists of a pure copper, as shown in drawing 3 (c), the upper copper film 207 is deposited on the lower layer copper film 206. In this case, as thickness of the lower layer copper film 206 and the upper copper film 207, it may be 925nm. Thereby, a contact hole 203 and the concave slot 204 for wiring are completely embedded by the copper films 206 and 207 of a lower layer and the upper layer.
[0053] Next, by the spatter, as shown in drawing 4 (a), the niobium film 208 which has 75nm thickness is deposited on the upper copper film 207.
[0054] Next, by performing heat treatment of about 400 degrees C in the reducing atmosphere containing hydrogen, and making the copper films 206 and 207 of a lower layer and the upper layer diffuse Nb of the niobium film 208, in order to prevent scaling of the niobium film 208, as shown in drawing 4 (b), the copper alloy film 209 which consists of Cu-7.2 % of the weight Nb is formed. In this case, the thickness of the copper films 206 and 207 of a lower layer and the upper layer is [the thickness of 925nm and the niobium film 208] 75nm, and since the consistency of Cu is 8.56, as for the copper alloy film 209, the consistency of 8.93 and Nb consists of Cu-7.2 % of the weight Nb based on the rate of the product of a volume ratio x consistency.
[0055] By the way, about the content of Nb in the copper alloy film 209, under the temperature of about 500 degrees C, the solid-solution limit of Nb in Cu is about 0.4 % of the weight, and when Nb is made to contain more than it, it has a possibility of depositing locally [the phase which uses Nb as a principal component] in the copper alloy film 209. Therefore, considering being 500 degrees C or less, the temperature of heat treatment in a semi-conductor process has 0.4 or less desirable % of the weight as a content of Nb.
[0056] Next, by performing the CMP method as opposed to the TiN/Ti film 205 and the copper alloy film 209, and removing the TiN/Ti film 205 and the copper alloy film 209 which have been exposed on an interlayer insulation film 202, as shown in drawing 4 (c), the contact 210 and the embedding wiring 211 which consist of copper alloy film 209 are formed. Then, it continues on the embedding wiring 211 and an interlayer insulation film 202 on the whole surface, and the silicon nitride film 212 which prevents the diffusion to the upper part of Cu which constitutes the embedding wiring 211 is deposited.
[0057] The conductivity of the copper alloy film 209 which consists of Cu-7.2 % of the weight Nb is 2.0microohm-cm extent [a little] higher than a pure copper (KR.Karasek et al., J.Appl.Phys.52 (1991), 1370). And as shown in the property Fig. of drawing 8 , it is thought that the Cu-Nb film has large tensile strength, and electromigration resistance also becomes strong. Therefore, it consists of copper alloy film 209, and embeds, and wiring 211 is excellent in both conductivity and electromigration resistance.
[0058] Since the niobium film 208 is deposited on the copper film 207 of the flat upper layer deposited with a CVD method or plating excellent in step coverage nature and thickness of the niobium film 208 can be enlarged, the copper films 206 and 207 of a lower layer and the upper layer can be made to diffuse certainly Nb which constitutes the niobium film 208 in the 2nd operation gestalt.
[0059] In addition, in the 2nd operation gestalt, although the copper alloy film 209 which Cu which constitutes the copper films 206 and 207 of a lower layer and the upper layer, and Nb which constitutes the niobium film 208 are made to react nearly completely, and consists of Cu-7.2 % of the weight Nb was formed, even if it replaces with this and makes it the niobium film 208 remain after heat treatment, this niobium film 208 is removable with the copper alloy film 209 by the CMP method.

[0060] Moreover, if the front face of an interlayer insulation film 202 and the semi-conductor substrate 201 is processed with the ammonia plasma etc. and diffusion of Cu is prevented, it is not necessary to deposit diffusion prevention film like the TiN/Ti film 205.
[0061] (3rd operation gestalt) Copper alloy wiring in the semiconductor device concerning the 3rd operation gestalt of this invention and its manufacture approach are explained hereafter, referring to drawing 5 (a) - (d) and drawing 6 (a) - (c).
[0062] First, as shown in drawing 5 (a), a contact hole 303 and the concave slot 304 for wiring are formed in the interlayer insulation film 302 deposited on the semi-conductor substrate 301. The path of a contact hole 303 may be about 0.25 micrometers.
[0063] Next, as shown in drawing 5 (b), it continues on the whole surface on the interlayer insulation film 302 including a contact hole 303 and the concave slot 304 for wiring, and the TiN/Ti film 305 which consists of the upper TiN film which prevents the diffusion to lower layer Ti film, the interlayer insulation film 302 of Cu, and the semi-conductor substrate 301 which raise adhesion with the semi-conductor substrate 301 is deposited.
[0064] Next, with a CVD method or plating, after depositing the lower layer copper film 306 on the TiN/Ti film 305 by the spatter, as shown in drawing 5 (c), the upper copper film 307 is deposited on the lower layer copper film 306. Thereby, a contact hole 303 and the concave slot 304 for wiring are completely embedded by the copper films 306 and 307 of a lower layer and the upper layer.
[0065] Next, the CMP method is performed as opposed to the copper films 306 and 307 of the TiN/Ti film 305, a lower layer, and the upper layer, and after removing the copper films 306 and 307 of the TiN/Ti film 305 exposed on an interlayer insulation film 302, a lower layer, and the upper layer, as wet etching by the nitric acid is performed to the upper copper film 307 and it is shown in drawing 5 (d), the space section is formed on the upper copper film 307.
[0066] Next, by a nonelectrolytic plating method etc., as shown in drawing 6 (a), a silver film 308 is alternatively deposited on the upper copper film 307.
[0067] Next, while forming the copper alloy film 309 which consists of Ag Cu-0.1% of the weight as by performing heat treatment of about 400 degrees C in the reducing atmosphere containing hydrogen, and making the copper films 306 and 307 of a lower layer and the upper layer diffuse Ag of a silver film 308 shows to drawing 6 (b) in order to prevent scaling of a silver film 308, the contact 310 and the embedding wiring 311 which consist of this copper alloy film 309 are formed. In this case, the thickness of the copper films 306 and 307 of a lower layer and the upper layer and a silver film 308 is adjusted so that the copper alloy film 309 which consists of Ag Cu-0.1% of the weight may be formed.
[0068] Next, as shown in drawing 6 (c), it continues on the embedding wiring 311 and an interlayer insulation film 302 on the whole surface, and the silicon nitride film 312 which prevents the diffusion to the upper part of Cu which constitutes the embedding wiring 311 is deposited.
[0069] Since the field made to react by heat treatment is restricted to the upper copper film 307 and the silver film 308 deposited alternatively according to the 3rd operation gestalt, the process which removes the film deposited on the interlayer insulation film 302 by the CMP method becomes easy.
[0070] In addition, in the 3rd operation gestalt, although the silver film 308 was alternatively deposited on the upper copper film 307, it replaces with this, and after covering the whole surface and depositing a silver film 308, heat treatment may be performed, the copper alloy film 309 may be formed, and the silver film 308 which remains may be removed by the CMP method after that.
[0071] (4th operation gestalt) Copper alloy wiring in the semiconductor device concerning the 4th operation gestalt of this invention and its manufacture approach are explained hereafter, referring to drawing 7 (a) - (c).
[0072] First, after forming a contact hole and the concave slot for wiring in the interlayer insulation film 402 deposited on the semi-conductor substrate 401 like the 3rd operation gestalt, on the interlayer insulation film 402 including a contact hole and the concave slot for wiring, the whole surface is covered and the TiN/Ti film 405 is deposited. After depositing the lower layer copper film 406 on the TiN/Ti film 405 by the spatter, with next, a CVD method or plating As the upper copper film 407 is deposited on the lower layer copper film 406, and the CMP method is performed after that as opposed to the

copper films 406 and 407 of the TiN/Ti film 405, a lower layer, and the upper layer and it is shown in drawing 7 (a) The copper films 406 and 407 of the TiN/Ti film 405 exposed on an interlayer insulation film 402, a lower layer, and the upper layer are removed.
[0073] Next, as shown in drawing 7 (b), on the upper copper film 407 and an interlayer insulation film 402, the whole surface is covered and the alumina film 408 is deposited.
[0074] Next, aluminum 2O3 which heat-treats and constitutes the alumina film 408 As the copper films 406 and 407 of a lower layer and the upper layer are diffused and it is shown in drawing 7 (c), it is Cu-aluminum 2O3. While forming the becoming copper alloy film 409, the contact 410 and the embedding wiring 411 which consist of this copper alloy film 409 are formed.
[0075] Since the alumina film 408 can be used as an interlayer insulation film while not removing, since the alumina film 408 has insulation according to the 4th operation gestalt, reduction of a routing counter can be aimed at.
[0076] in addition, the 1- in the 4th operation gestalt, although the pure copper was used as copper films 107, 207, 307, and 407, it may replace with this and the copper alloy with which it comes to contain other metals in Cu may be used.
[0077] Moreover, the TiN/Ti film 105, 205, 305, and 405 or copper films 107, 207, 307, and 407 may be deposited only on the interior of contact holes 103, 203, and 303 and the concave slots 104, 204, and 304 for wiring with a selection CVD method, and other diffusion prevention film, for example, Ta film, TaN film, or WN film etc. may be used instead of the TiN/Ti film 105, 205, 305, and 405.
[0078] Moreover, if the embedding inside contact holes 103, 203, and 303 and the concave slots 104, 204, and 304 for wiring is possible, copper films 107, 207, and 307 may be formed by other approaches, such as the spatter + reflow method or the ion plating method.
[0079] Furthermore, in case the upper copper films 207, 307, and 407 are deposited, when you do not need the copper film of a substrate, you may omit the lower layer copper films 206, 306, and 406.
[0080]
[Effect of the Invention] Since according to the 1st semiconductor device the Cu-Nb alloy, the Cu-Ag alloy, or 2OCu-aluminum3 alloy which constitutes embedding wiring reaches in tension strength, and is excellent in both conductivity and it can raise both the conductivity of embedding wiring, and electromigration resistance, the dependability of a semiconductor device improves.
[0081] In the 1st semiconductor device, the phase which uses Ag as a principal component in heat treatment of 500 degrees C or less in a semi-conductor process when 1 or less % of the weight of Ag comes for a copper alloy to contain in Cu can avoid the situation where embed with a sludge since it does not deposit locally in a copper alloy, and the conductivity of wiring varies.
[0082] Moreover, in the 1st semiconductor device, the phase which uses Nb as a principal component in heat treatment of 500 degrees C or less in a semi-conductor process when 0.4 or less % of the weight of Nb comes for a copper alloy to contain in Cu can avoid the situation where embed with a sludge since it does not deposit locally in a copper alloy, and the conductivity of wiring varies.
[0083] According to the 2nd semiconductor device, like the 1st semiconductor device, while being able to raise both the conductivity of embedding wiring, and electromigration resistance, it can use effectively as the source of supply and insulator layer of aluminum 2O3 which embeds the insulator layer containing aluminum 2O3, and wiring is made to diffuse.
[0084] according to the manufacture approach of the 1st semiconductor device -- Cu -- Ag, Nb, or aluminum 2O3 it consists of a contained copper alloy -- embedding -- wiring -- DAMASHIN -- law or dual DAMASHIN -- it can form certainly by law.
[0085] In the manufacture approach of the 1st semiconductor device, after covering the whole surface and depositing the 1st metal membrane on an interlayer insulation film, on this 1st metal membrane, the whole surface is covered, the 2nd metal membrane is deposited, and if the 1st metal membrane and 2nd metal membrane which have been exposed on an interlayer insulation film are removed after that, embedding wiring can be formed simply and certainly.
[0086] In the manufacture approach of the 1st semiconductor device, if the 2nd metal membrane is deposited with a CVD method or plating after depositing the 1st metal membrane by the spatter, the 1st

and 2nd metal membranes can be embedded certainly also in the high crevice for wiring of an aspect ratio.

[0087] According to the manufacture approach of the 2nd semiconductor device, they are Ag, Nb, or aluminum 2O3 to Cu. While being able to consist of a contained copper alloy, being able to embed and being able to form wiring certainly Since the front face of the 2nd metal membrane is almost flat, CMP can remove the 1st metal membrane and 2nd metal membrane which have been exposed on an interlayer insulation film, and the process which embeds in the crevice for wiring and forms wiring can be performed easily and certainly.

[0088] According to the manufacture approach of the 3rd semiconductor device, they are Ag, Nb, or aluminum 2O3 to Cu. Since the process which removes the 1st and 2nd metal membranes which consist of a contained copper alloy, and which were exposed on the interlayer insulation film becomes unnecessary while being able to embed and being able to form wiring certainly, without causing the increment in a routing counter, it can consist of a copper alloy, and can embed and wiring can be formed.

[0089] According to the manufacture approach of the 4th semiconductor device, they are Ag, Nb, or aluminum 2O3 to Cu. While being able to embed and being able to form wiring certainly, since the front face of the 2nd metal membrane is almost flat, CMP can remove the 2nd metal membrane which consists of a contained copper alloy and which has been exposed on an interlayer insulation film, and the process which embeds in the crevice for wiring and forms wiring can be performed easily and certainly. When insulating aluminum 2O3 is used as the 2nd metal membrane, it can use as an insulator layer, without removing the 2nd metal membrane.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the semiconductor device which has embedding wiring, and its manufacture approach.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] In LSI formed on the silicon substrate after 0.18-micrometer generation, since it is impossible to disregard delay by CR component of wiring to improvement in the speed of a transistor, it is desirable to use a conductive high metal, i.e., the small metal of specific resistance, as a wiring material. then, aluminum wiring (3micro ohm-cm of specific resistance) -- replacing with -- more -- low -- the examination using Cu wiring [****] (1.7micro ohm-cm of specific resistance) is progressing.
[0003] Moreover, since the consistency of the flowing current is increasing metal wiring for every generation with detailed-izing of the component which constitutes LSI, the metal atom which constitutes metal wiring at the time of current impression needs to be pushed on an electron, needs to move, and it is necessary to raise the resistance also to the phenomenon of the electromigration which metal wiring disconnects. It is expected that it will be expected that deformation, i.e., migration of an atom, cannot take place easily since the melting point is high compared with aluminum, and electromigration resistance of Cu will also be high.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] Since according to the 1st semiconductor device the Cu-Nb alloy, the Cu-Ag alloy, or 2OCu-aluminum3 alloy which constitutes embedding wiring reaches in tension strength, and is excellent in both conductivity and it can raise both the conductivity of embedding wiring, and electromigration resistance, the dependability of a semiconductor device improves.
[0081] In the 1st semiconductor device, the phase which uses Ag as a principal component in heat treatment of 500 degrees C or less in a semi-conductor process when 1 or less % of the weight of Ag comes for a copper alloy to contain in Cu can avoid the situation where embed with a sludge since it does not deposit locally in a copper alloy, and the conductivity of wiring varies.
[0082] Moreover, in the 1st semiconductor device, the phase which uses Nb as a principal component in heat treatment of 500 degrees C or less in a semi-conductor process when 0.4 or less % of the weight of Nb comes for a copper alloy to contain in Cu can avoid the situation where embed with a sludge since it does not deposit locally in a copper alloy, and the conductivity of wiring varies.
[0083] According to the 2nd semiconductor device, like the 1st semiconductor device, while being able to raise both the conductivity of embedding wiring, and electromigration resistance, it can use effectively as the source of supply and insulator layer of aluminum 2O3 which embeds the insulator layer containing aluminum 2O3, and wiring is made to diffuse.
[0084] according to the manufacture approach of the 1st semiconductor device -- Cu -- Ag, Nb, or aluminum 2O3 it consists of a contained copper alloy -- embedding -- wiring -- DAMASHIN -- law or dual DAMASHIN -- it can form certainly by law.
[0085] In the manufacture approach of the 1st semiconductor device, after covering the whole surface and depositing the 1st metal membrane on an interlayer insulation film, on this 1st metal membrane, the whole surface is covered, the 2nd metal membrane is deposited, and if the 1st metal membrane and 2nd metal membrane which have been exposed on an interlayer insulation film are removed after that, embedding wiring can be formed simply and certainly.
[0086] In the manufacture approach of the 1st semiconductor device, if the 2nd metal membrane is deposited with a CVD method or plating after depositing the 1st metal membrane by the spatter, the 1st and 2nd metal membranes can be embedded certainly also in the high crevice for wiring of an aspect ratio.
[0087] According to the manufacture approach of the 2nd semiconductor device, they are Ag, Nb, or aluminum 2O3 to Cu. While being able to consist of a contained copper alloy, being able to embed and being able to form wiring certainly, Since the front face of the 2nd metal membrane is almost flat, CMP can remove the 1st metal membrane and 2nd metal membrane which have been exposed on an interlayer insulation film, and the process which embeds in the crevice for wiring and forms wiring can be performed easily and certainly.
[0088] According to the manufacture approach of the 3rd semiconductor device, they are Ag, Nb, or aluminum 2O3 to Cu. Since the process which removes the 1st and 2nd metal membranes which consist of a contained copper alloy, and which were exposed on the interlayer insulation film becomes unnecessary while being able to embed and being able to form wiring certainly, without causing the

increment in a routing counter, it can consist of a copper alloy, and can embed and wiring can be formed.

[0089] According to the manufacture approach of the 4th semiconductor device, they are Ag, Nb, or aluminum 2O3 to Cu. While being able to embed and being able to form wiring certainly, since the front face of the 2nd metal membrane is almost flat, CMP can remove the 2nd metal membrane which consists of a contained copper alloy and which has been exposed on an interlayer insulation film, and the process which embeds in the crevice for wiring and forms wiring can be performed easily and certainly. When insulating aluminum 2O3 is used as the 2nd metal membrane, it can use as an insulator layer, without removing the 2nd metal membrane.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, although metal wiring which consists of Cu is extremely excellent about conductivity, if wiring width of face becomes more detailed, it will be considered that a problem remains in respect of electromigration resistance. For example, it is reported by detailed metal wiring about 0.3-micrometer width of face that electromigration resistance gets worse [Y.Igarashi et al, VLSI Symp., p.76, and 1996]. Therefore, raising electromigration resistance by alloying is examined like the case of aluminum wiring.

[0005] Then, the Cu-Mg alloy [T.Tatewaki et al, IEDM., p.293, and 1995], the Cu-Zr alloy [Y.Igarashi et al, VLSI Symp., p.76, and 1996], the Cu-Sn alloy, etc. are proposed as a wiring material.

[0006] However, although wiring which consists of copper alloys, such as a Cu-Mg alloy, a Cu-Zr alloy, or a Cu-Sn alloy, is excellent in respect of electromigration resistance, a problem remains in respect of conductivity.

[0007] In view of the above, this invention aims at offering the semiconductor device excellent in conductivity and electromigration resistance with the high dependability which embeds and has wiring by offering the wiring material which can aim at coexistence with improvement in conductivity, and improvement in electromigration resistance.

[Translation done.]

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MEANS

[Means for Solving the Problem] The ingredient of tension strength with a large invention-in-this-application person thought that it should excel also in electromigration resistance. As a result which the copper atom which constitutes copper alloy wiring moves, when a current is passed to copper alloy wiring, while compressive stress increases, tensile stress occurs in the part to which copper atoms decreased in number, and copper alloy wiring disconnects the reason in the part to which copper atoms decreased in number by the part which the copper atom increased. Therefore, the copper alloy with large tension strength must be excellent in electromigration resistance. Then, when the copper alloy which reached in tension strength and was excellent in both conductivity was used as a wiring material, the conclusion that copper alloy wiring with the high dependability excellent in conductivity and electromigration resistance should be obtained was reached.
[0009] When searched for the copper alloy which reached in tension strength among various kinds of copper alloys, and was excellent in both conductivity, the data (wait ****, p.692, 1997 besides Sakai) shown in drawing 8 were found out. According to the property Fig. shown in drawing 8 , the Cu-Nb alloy, the Cu-Ag alloy, and 2OCu-aluminum3 alloy found out that it was the copper alloy which reached in tension strength among various kinds of copper alloys, and was excellent in both conductivity. In addition, in drawing 8 , %IACS shows the rate of conductivity to the conductivity of a pure copper.
[0010] If it embeds using the copper alloy with which Nb, Ag, or aluminum 2O3 was contained in Cu and wiring is formed so that the above examination may show, a semiconductor device with the high dependability excellent in conductivity and electromigration resistance will be obtained.
[0011] Embedding wiring is Ag, Nb, or aluminum 2O3 to Cu for the semiconductor device with which the 1st semiconductor device concerning this invention has embedding wiring. It consists of a contained copper alloy.
[0012] According to the 1st semiconductor device, embedding wiring is set to Cu from the Cu-Nb alloy, the Cu-Ag alloy, or 2OCu-aluminum3 alloy which Ag, Nb, or aluminum 2O3 comes to contain, and as shown in the property Fig. of drawing 8 , these Cu-Nb alloy, a Cu-Ag alloy, and 2OCu-aluminum3 alloy reach in tension strength, and are excellent in both conductivity.
[0013] As for a copper alloy, in the 1st semiconductor device, it is desirable that 1 or less % of the weight of Ag comes to contain in Cu.
[0014] Moreover, as for a copper alloy, in the 1st semiconductor device, it is desirable that 0.4 or less % of the weight of Nb comes to contain in Cu.
[0015] An insulator layer contains aluminum 2O3 for the semiconductor device which has the insulator layer by which the 2nd semiconductor device concerning this invention was formed after embedding wiring and this embedding wiring, and embedding wiring is set to Cu from the copper alloy which aluminum 2O3 comes to spread.
[0016] According to the 2nd semiconductor device, embedding wiring is set to Cu from 2OCu-aluminum3 alloy which aluminum 2O3 comes to contain, and as shown in the property Fig. of drawing 8 , this 2OCu-aluminum3 alloy reaches in tension strength, and is excellent in both conductivity. Moreover, since the insulator layer formed after embedding wiring contains aluminum 2O3, it embeds

aluminum 2O3 contained in an insulator layer, and wiring is made to diffuse it, and it can form easily in Cu 2OCu-aluminum3 alloy which aluminum 2O3 comes to contain. In this case, since aluminum 2O3 has insulation, it can also be used as an insulator layer as it is.
[0017] The manufacture approach of the 1st semiconductor device concerning this invention The crevice formation process which forms the crevice for wiring in the interlayer insulation film deposited on the semi-conductor substrate, They are Ag, Nb, or aluminum 2O3 to Cu in the wall surface of the crevice for wiring. The 1st metal membrane formation process which forms the 1st metal membrane which consists of the 1st contained metal, The 2nd metal membrane formation process which forms the 2nd metal membrane which consists of the 2nd metal which uses Cu or Cu as a principal component on the 1st metal membrane so that the crevice for wiring may be embedded, Ag, Nb, or aluminum 2O3 which heat-treats to a semi-conductor substrate and is contained in the 1st metal membrane By diffusing the 2nd metal membrane It has the embedding wiring formation process which is set to Cu from the copper alloy which Ag, Nb, or aluminum 2O3 contained and which embeds and forms wiring.
[0018] According to the manufacture approach of the 1st semiconductor device, at Cu on the wall surface of the crevice for wiring formed in the interlayer insulation film Ag, Nb or aluminum 2O3 After forming the 1st metal membrane which consists of the 1st contained metal, Ag, Nb, or aluminum 2O3 which forms the 2nd metal membrane which consists of the 2nd metal which uses Cu or Cu as a principal component on this 1st metal membrane, performs heat treatment after that, and is contained in the 1st metal membrane Since the 2nd metal membrane is diffused, They are Ag, Nb, or aluminum 2O3 to Cu. It can consist of a contained copper alloy, and can embed, and wiring can be formed.
[0019] Since the metal membrane of the copper system which uses Cu or Cu as a principal component is difficult dry etching, by the way, embedding wiring DAMASHIN which embeds the metal membrane of a copper system in the crevice for wiring since the crevice for wiring is formed in the interlayer insulation film -- according to the manufacture approach of the 1st semiconductor device, although formed of law in many cases it is set to Cu from the copper alloy which Ag, Nb, or aluminum 2O3 contained -- embedding -- wiring -- DAMASHIN -- it can form by law. Moreover, since the contact hole is formed in the crevice bottom for wiring, if a metal membrane is embedded in both a contact hole and the crevice for wiring at coincidence, the contact and embedding wiring which consist of a copper alloy by the dual DAMASHIN method can be formed in coincidence.
[0020] In the manufacture approach of the 1st semiconductor device the 1st metal membrane formation process The process which covers the whole surface and deposits the 1st metal membrane on an interlayer insulation film including the crevice for wiring is included. The 2nd metal membrane formation process It is desirable to include the process which removes the 1st metal membrane and 2nd metal membrane which have exposed the embedding wiring formation process on an interlayer insulation film including the process which covers the whole surface and deposits the 2nd metal membrane on the 1st metal membrane.
[0021] In the manufacture approach of the 1st semiconductor device, it is desirable to include the process on which the 2nd metal membrane formation process deposits the 2nd metal membrane with a CVD method or plating including the process on which the 1st metal membrane formation process deposits the 1st metal membrane by the spatter.
[0022] By the way, in the generation whose design rule is 0.18 micrometers, a contact hole is a diameter of 0.25 micrometer, and it becomes a depth of about 0.8 micrometers, and it is predicted that a depth of about 0.5 micrometers is needed also about the crevice for wiring. If it is going to form such detailed wiring structure using the dual DAMASHIN method, the depth needs to embed a copper alloy by about 1.3 micrometers at the hole (hole whose aspect ratio is about five) whose path is about 0.25 micrometers. However, according to the present technique, in a CVD method and plating, although the metal membrane of a pure copper can be deposited, the metal membrane of a copper alloy cannot be deposited. Moreover, according to the spatter, the metal membrane of a copper alloy can be deposited, but since an overhang will be generated if it is going to deposit on the high crevice for wiring of an aspect ratio, it is difficult [it] to embed a metal membrane by the spatter in the high crevice for wiring which is an aspect ratio.

[0023] However, if the process on which the 2nd metal membrane formation process deposits the 2nd metal membrane with a CVD method or plating is included including the process on which the 1st metal membrane formation process deposits the 1st metal membrane by the spatter After forming the 1st metal membrane which becomes the wall surface of the crevice for wiring from the 1st metal which Ag, Nb, or aluminum 2O3 contained in Cu by the spatter, Since the 2nd metal membrane which consists of the 2nd metal which uses Cu or Cu as a principal component is deposited with a CVD method or plating excellent in step coverage nature, the 1st metal membrane and 2nd metal membrane can be embedded in the crevice for wiring.

[0024] The manufacture approach of the 2nd semiconductor device concerning this invention The crevice formation process which forms the crevice for wiring in the interlayer insulation film deposited on the semi-conductor substrate, The 1st metal membrane formation process which continues and forms in the whole surface the 1st metal membrane which consists of the 1st metal which uses Cu or Cu as a principal component on an interlayer insulation film including the crevice for wiring so that the crevice for wiring may be embedded, They are Ag, Nb, or aluminum 2O3 on the 1st metal membrane. The 2nd metal membrane formation process which forms the 2nd metal membrane which consists of the 2nd metal to contain, Ag, Nb, or aluminum 2O3 which heat-treats to a semi-conductor substrate and is contained in the 2nd metal membrane The diffusion process which the 1st metal membrane is made to diffuse, The 1st metal membrane and 2nd metal membrane which have been exposed on an interlayer insulation film are removed, and they are Ag, Nb, or aluminum 2O3 to Cu. It has the embedding wiring formation process which consists of a contained copper alloy and which embeds and forms wiring.

[0025] After forming the 1st metal membrane which consists of the 1st metal which uses Cu or Cu as a principal component on an interlayer insulation film including the crevice for wiring formed in the interlayer insulation film according to the manufacture approach of the 2nd semiconductor device, They are Ag, Nb, or aluminum 2O3 on this 1st metal membrane. The 2nd metal membrane which consists of the 2nd metal to contain is formed. Then, Ag, Nb, or aluminum 2O3 which is heat-treated and is contained in the 2nd metal membrane Since the 1st metal membrane is diffused, they are Ag, Nb, or aluminum 2O3 to Cu. It can consist of a contained copper alloy, and can embed, and wiring can be formed.

[0026] After especially the manufacture approach of the 2nd semiconductor device covers the whole surface and forms the 1st metal membrane so that the crevice for wiring may be embedded, in order that it may form the 2nd metal membrane on this 1st metal membrane, the front face of the 2nd metal membrane is almost flat. Therefore, the 2nd Ag, Nb, or aluminum 2O3 from a metal membrane It can be spread more to homogeneity.

[0027] The manufacture approach of the 3rd semiconductor device concerning this invention The crevice formation process which forms the crevice for wiring in the interlayer insulation film deposited on the semi-conductor substrate, The 1st metal membrane formation process which forms the 1st metal membrane which becomes a crevice for wiring from the 1st metal which uses Cu or Cu as a principal component so that the space section may remain on this 1st metal membrane, They are Ag, Nb, or aluminum 2O3 on the 1st metal membrane. The 2nd metal membrane formation process which forms the 2nd metal membrane which consists of the 2nd contained metal so that the space section may be embedded and it may not expose on an interlayer insulation film, Ag, Nb, or aluminum 2O3 which heat-treats to a semi-conductor substrate and is contained in the 2nd metal membrane By diffusing the 1st metal membrane They are Ag, Nb, or aluminum 2O3 to Cu. It has the embedding wiring formation process which consists of a contained copper alloy and which embeds and forms wiring.

[0028] After forming the 1st metal membrane which consists of the 1st metal which uses Cu or Cu as a principal component in the crevice for wiring formed in the interlayer insulation film according to the manufacture approach of the 3rd semiconductor device, They are Ag, Nb, or aluminum 2O3 on this 1st metal membrane. The 2nd metal membrane which consists of the 2nd contained metal is formed. Then, Ag, Nb, or aluminum 2O3 which is heat-treated and is contained in the 2nd metal membrane Since the 1st metal membrane is diffused, they are Ag, Nb, or aluminum 2O3 to Cu. It can consist of a contained copper alloy, and can embed, and wiring can be formed.

[0029] After forming the 1st metal membrane in the crevice for wiring especially according to the manufacture approach of the 3rd semiconductor device so that the space section may remain at this 1st metal membrane top, Since it forms so that the space section may be embedded in the 2nd metal membrane on this 1st metal membrane and it may not expose on an interlayer insulation film, and heat treatment is performed after that, the process which removes the 1st and 2nd metal membranes exposed on the interlayer insulation film becomes unnecessary.
[0030] The manufacture approach of the 4th semiconductor device concerning this invention The crevice formation process which forms the crevice for wiring in the interlayer insulation film deposited on the semi-conductor substrate, The 1st metal membrane formation process which forms the 1st metal membrane which becomes a crevice for wiring from the 1st metal which uses Cu or Cu as a principal component so that the crevice for wiring may be embedded and it may not expose on an interlayer insulation film, They are Ag, Nb, or aluminum 2O3 on the 1st metal membrane. The 2nd metal membrane formation process which forms the 2nd metal membrane which consists of the 2nd metal to contain, Ag, Nb, or aluminum 2O3 which heat-treats to a semi-conductor substrate and is contained in the 2nd metal membrane By diffusing the 1st metal membrane They are Ag, Nb, or aluminum 2O3 to Cu. It has the embedding wiring formation process which consists of a contained copper alloy and which embeds and forms wiring.
[0031] After forming the 1st metal membrane which consists of the 1st metal which uses Cu or Cu as a principal component in the crevice for wiring formed in the interlayer insulation film according to the manufacture approach of the 4th semiconductor device, They are Ag, Nb, or aluminum 2O3 on this 1st metal membrane. The 2nd metal membrane which consists of the 2nd metal to contain is formed. Then, Ag, Nb, or aluminum 2O3 which is heat-treated and is contained in the 2nd metal membrane Since the 1st metal membrane is diffused, they are Ag, Nb, or aluminum 2O3 to Cu. It can consist of a contained copper alloy, and can embed, and wiring can be formed.
[0032] After forming so that the crevice for wiring may be embedded in the 1st metal membrane in the crevice for wiring and it may not expose on an interlayer insulation film, in order to form the 2nd metal membrane on this 1st metal membrane especially according to the manufacture approach of the 4th semiconductor device, the front face of the 2nd metal membrane is almost flat.
[0033]
[Embodiment of the Invention] (1st operation gestalt) Copper alloy wiring in the semiconductor device concerning the 1st operation gestalt of this invention and its manufacture approach are explained hereafter, referring to drawing 1 (a) - (c) and drawing 2 (a), and (b).
[0034] First, as shown in drawing 1 (a), a contact hole 103 and the concave slot 104 for wiring are formed in the interlayer insulation film 102 deposited on the semi-conductor substrate 101. The path of a contact hole 103 may be about 0.25 micrometers.
[0035] Next, as shown in drawing 1 (b), it continues on the whole surface on the interlayer insulation film 102 including a contact hole 103 and the concave slot 104 for wiring, and the TiN/Ti film 105 which consists of the upper TiN film which prevents the diffusion to lower layer Ti film, the interlayer insulation film 102 of Cu, and the semi-conductor substrate 101 which raise adhesion with the semi-conductor substrate 101 is deposited.
[0036] Next, the copper alloy film 106 which has 40nm thickness is deposited on the TiN/Ti film 105 by the spatter using the target of the copper alloy which consists of Ag Cu-1% of the weight. In this case, since step coverage nature of a spatter generally is not good, the small contact hole 103 of an about 0.25-micrometer diameter and the concave slot 104 for wiring cannot be completely embedded with the copper alloy film 106. The reason is that the copper alloy film 106 will overhang [near the opening of the small contact hole 103 of a path] if the copper alloy film 106 is deposited by the spatter.
[0037] Then, the CVD method or plating which was excellent in step coverage nature after the aforementioned spatter is performed, and as shown in drawing 1 (c), the copper film 107 which has the film 106 (480nm) about 11 times the thickness of a copper alloy is deposited on the copper alloy film 106. Thereby, a contact hole 103 and the concave slot 104 for wiring are completely embedded by the copper alloy film 106 and the copper film 107. the case where electrolytic plating is used as plating in

order to raise surface surface smoothness in the CVD method of Cu -- a substrate -- low -- since Cu film [****] is required, in a CVD method or plating, it is required to use the copper alloy film 106 for a substrate.

[0038] Next, by performing heat treatment of about 400 degrees C, and making the Cu film 107 diffuse Ag of the copper alloy film 106, as shown in drawing 2 (a), the copper alloy film 108 which consists of Ag Cu-0.085% of the weight is formed.

[0039] By the way, about the content of Ag in the copper alloy film 108, under the temperature of about 500 degrees C, the solid-solution limit of Ag in Cu is about 1 % of the weight, and when Ag is made to contain more than it, it has a possibility of depositing locally [the phase which uses Ag as a principal component] in the copper alloy film 108. Therefore, considering being 500 degrees C or less, the temperature of heat treatment in a semi-conductor process has 1 or less desirable % of the weight as a content of Ag.

[0040] Next, by performing the CMP method as opposed to the TiN/Ti film 105 and the copper alloy film 108, and removing the TiN/Ti film 105 and the copper alloy film 108 which have been exposed on an interlayer insulation film 102, as shown in drawing 2 (b), the contact 109 and the embedding wiring 110 which consist of copper alloy film 108 are formed. Then, it continues on the embedding wiring 110 and an interlayer insulation film 102 on the whole surface, and the silicon nitride film 111 which prevents the diffusion to the upper part of Cu which constitutes the embedding wiring 110 is deposited.

[0041] The recrystallizing temperature of the copper alloy film 108 which consists of Cu-0.085-% of the weight Ag formed in the 1st operation gestalt is higher than 250 degrees C which is the recrystallizing temperature of a pure copper, and is 400 degrees C (1223 the Japan Institute of Metals besides a ditch, p 1981). Since I hear that it is hard to deform that recrystallizing temperature is high plastically, it is and a hillock and a void cannot produce the copper alloy film 108 easily, it is proved that electromigration resistance improves.

[0042] Moreover, in the copper alloy film 108 which consists of Ag Cu-0.085% of the weight, since the concentration of Ag is about 50 ppm, the conductivity of the copper alloy film 108 is 1.7microohm-cm almost equivalent to a pure copper (J. S.Smart et al., Trans.AIME, 147 (1942), 48). Therefore, the conductivity of the copper alloy film 108 does not fall compared with a pure copper. On the other hand, if it consists of Cu-Zr alloy film already known, it embeds and about 50 ppm of Zr are added in wiring, while electrical conductivity will rise to 2.2microohm-cm, Zr and Cu react, and it is CuZrx. Since there is a problem of being easy to make a compound, the copper alloy film 108 which consists of Cu-Ag is more advantageous like the 1st operation gestalt.

[0043] As explained above, it consists of copper alloy film 108, and embeds, and wiring 110 is excellent in both conductivity and electromigration resistance.

[0044] By the way, with the present technique, while being unable to deposit the copper alloy film which consists of Cu-Ag with a CVD method or plating, the copper alloy film cannot be completely embedded by the spatter in the small contact hole of a path. Then, in the 1st operation gestalt, while depositing thinly the copper alloy film 106 which consists of Ag Cu-1% of the weight by the spatter, after depositing a copper film 107 thickly with a CVD method or plating on the copper alloy film 106, the copper alloy film 108 which consists of Ag Cu-0.085% of the weight is formed by performing heat treatment and making a copper film 107 diffuse Ag of the copper alloy film 106.

[0045] Moreover, since the copper alloy film 106 deposited by the spatter has the property which carries out orientation in a field (111), it carries out orientation of the copper film 107 deposited with a CVD method or plating on the copper alloy film 106 to a field (111) in response to the effect of a substrate. Therefore, field Uchihara child spacing can deposit the copper film 107 almost equal to the field (111) of the copper alloy film 106 with a CVD method or plating. Moreover, since Cu is the same fcc crystal as aluminum, the field which is the maximum **** (111) tends to serve as a cause of an open circuit, but since the field (111) of a copper film 107 is carrying out orientation to parallel with the principal plane of the semi-conductor substrate 11, it embeds, and it is hard coming to disconnect wiring 110, and it also has the advantage which consists of copper alloy film 108 that electromigration resistance improves further.

[0046] In addition, the copper alloy film 106 and copper film 107 which consist of Ag Cu-1% of the weight are made to react nearly completely, and the TiN film of the upper layer which constitutes the TiN/Ti film 105 may be made to contain Ag in the 1st operation gestalt, although the copper alloy film 108 which consists of Ag Cu-0.085% of the weight was formed instead of depositing the copper alloy film 106 which consists of Ag Cu-1% of the weight. In this case, it is desirable on a film deposition process to constitute a copper film 107 from a copper film of the upper layer deposited with lower layer copper film, CVD method, or plating deposited by the spatter.
[0047] Moreover, if the front face of an interlayer insulation film 102 and the semi-conductor substrate 101 is processed with the ammonia plasma etc. and diffusion of Cu is prevented, it is not necessary to deposit diffusion prevention film like the TiN/Ti film 105.
[0048] Moreover, in the 1st operation gestalt, although the Cu-Ag alloy proposed newly was used as copper alloy film 106, when conductivity may become low somewhat, a Cu-Sn alloy, a Cu-Mg alloy, or a Cu-Zr alloy may be used.
[0049] (2nd operation gestalt) Copper alloy wiring in the semiconductor device concerning the 2nd operation gestalt of this invention and its manufacture approach are explained hereafter, referring to drawing 3 (a) - (c) and drawing 4 (a) - (c).
[0050] First, as shown in drawing 3 (a), a contact hole 203 and the concave slot 204 for wiring are formed in the interlayer insulation film 202 deposited on the semi-conductor substrate 201. The path of a contact hole 203 may be about 0.25 micrometers.
[0051] Next, as shown in drawing 3 (b), it continues on the whole surface on the interlayer insulation film 202 including a contact hole 203 and the concave slot 204 for wiring, and the TiN/Ti film 205 which consists of the upper TiN film which prevents the diffusion to lower layer Ti film, the interlayer insulation film 202 of Cu, and the semi-conductor substrate 201 which raise adhesion with the semi-conductor substrate 201 is deposited.
[0052] Next, with a CVD method or plating, after depositing the lower layer copper film 206 on the TiN/Ti film 205 by the spatter using the target which consists of a pure copper, as shown in drawing 3 (c), the upper copper film 207 is deposited on the lower layer copper film 206. In this case, as thickness of the lower layer copper film 206 and the upper copper film 207, it may be 925nm. Thereby, a contact hole 203 and the concave slot 204 for wiring are completely embedded by the copper films 206 and 207 of a lower layer and the upper layer.
[0053] Next, by the spatter, as shown in drawing 4 (a), the niobium film 208 which has 75nm thickness is deposited on the upper copper film 207.
[0054] Next, by performing heat treatment of about 400 degrees C in the reducing atmosphere containing hydrogen, and making the copper films 206 and 207 of a lower layer and the upper layer diffuse Nb of the niobium film 208, in order to prevent scaling of the niobium film 208, as shown in drawing 4 (b), the copper alloy film 209 which consists of Cu-7.2 % of the weight Nb is formed. In this case, the thickness of the copper films 206 and 207 of a lower layer and the upper layer is [the thickness of 925nm and the niobium film 208] 75nm, and since the consistency of Cu is 8.56, as for the copper alloy film 209, the consistency of 8.93 and Nb consists of Cu-7.2 % of the weight Nb based on the rate of the product of a volume ratio x consistency.
[0055] By the way, about the content of Nb in the copper alloy film 209, under the temperature of about 500 degrees C, the solid-solution limit of Nb in Cu is about 0.4 % of the weight, and when Nb is made to contain more than it, it has a possibility of depositing locally [the phase which uses Nb as a principal component] in the copper alloy film 209. Therefore, considering being 500 degrees C or less, the temperature of heat treatment in a semi-conductor process has 0.4 or less desirable % of the weight as a content of Nb.
[0056] Next, by performing the CMP method as opposed to the TiN/Ti film 205 and the copper alloy film 209, and removing the TiN/Ti film 205 and the copper alloy film 209 which have been exposed on an interlayer insulation film 202, as shown in drawing 4 (c), the contact 210 and the embedding wiring 211 which consist of copper alloy film 209 are formed. Then, it continues on the embedding wiring 211 and an interlayer insulation film 202 on the whole surface, and the silicon nitride film 212 which

prevents the diffusion to the upper part of Cu which constitutes the embedding wiring 211 is deposited.
[0057] The conductivity of the copper alloy film 209 which consists of Cu-7.2 % of the weight Nb is 2.0microohm-cm extent [a little] higher than a pure copper (KR.Karasek et al., J.Appl.Phys.52 (1991), 1370). And as shown in the property Fig. of drawing 8 , it is thought that the Cu-Nb film has large tensile strength, and electromigration resistance also becomes strong. Therefore, it consists of copper alloy film 209, and embeds, and wiring 211 is excellent in both conductivity and electromigration resistance.
[0058] Since the niobium film 208 is deposited on the copper film 207 of the flat upper layer deposited with a CVD method or plating excellent in step coverage nature and thickness of the niobium film 208 can be enlarged, the copper films 206 and 207 of a lower layer and the upper layer can be made to diffuse certainly Nb which constitutes the niobium film 208 in the 2nd operation gestalt.
[0059] In addition, in the 2nd operation gestalt, although the copper alloy film 209 which Cu which constitutes the copper films 206 and 207 of a lower layer and the upper layer, and Nb which constitutes the niobium film 208 are made to react nearly completely, and consists of Cu-7.2 % of the weight Nb was formed, even if it replaces with this and makes it the niobium film 208 remain after heat treatment, this niobium film 208 is removable with the copper alloy film 209 by the CMP method.
[0060] Moreover, if the front face of an interlayer insulation film 202 and the semi-conductor substrate 201 is processed with the ammonia plasma etc. and diffusion of Cu is prevented, it is not necessary to deposit diffusion prevention film like the TiN/Ti film 205.
[0061] (3rd operation gestalt) Copper alloy wiring in the semiconductor device concerning the 3rd operation gestalt of this invention and its manufacture approach are explained hereafter, referring to drawing 5 (a) - (d) and drawing 6 (a) - (c).
[0062] First, as shown in drawing 5 (a), a contact hole 303 and the concave slot 304 for wiring are formed in the interlayer insulation film 302 deposited on the semi-conductor substrate 301. The path of a contact hole 303 may be about 0.25 micrometers.
[0063] Next, as shown in drawing 5 (b), it continues on the whole surface on the interlayer insulation film 302 including a contact hole 303 and the concave slot 304 for wiring, and the TiN/Ti film 305 which consists of the upper TiN film which prevents the diffusion to lower layer Ti film, the interlayer insulation film 302 of Cu, and the semi-conductor substrate 301 which raise adhesion with the semi-conductor substrate 301 is deposited.
[0064] Next, with a CVD method or plating, after depositing the lower layer copper film 306 on the TiN/Ti film 305 by the spatter, as shown in drawing 5 (c), the upper copper film 307 is deposited on the lower layer copper film 306. Thereby, a contact hole 303 and the concave slot 304 for wiring are completely embedded by the copper films 306 and 307 of a lower layer and the upper layer.
[0065] Next, the CMP method is performed as opposed to the copper films 306 and 307 of the TiN/Ti film 305, a lower layer, and the upper layer, and after removing the copper films 306 and 307 of the TiN/Ti film 305 exposed on an interlayer insulation film 302, a lower layer, and the upper layer, as wet etching by the nitric acid is performed to the upper copper film 307 and it is shown in drawing 5 (d), the space section is formed on the upper copper film 307.
[0066] Next, by a nonelectrolytic plating method etc., as shown in drawing 6 (a), a silver film 308 is alternatively deposited on the upper copper film 307.
[0067] Next, while forming the copper alloy film 309 which consists of Ag Cu-0.1% of the weight as by performing heat treatment of about 400 degrees C in the reducing atmosphere containing hydrogen, and making the copper films 306 and 307 of a lower layer and the upper layer diffuse Ag of a silver film 308 shows to drawing 6 (b) in order to prevent scaling of a silver film 308, the contact 310 and the embedding wiring 311 which consist of this copper alloy film 309 are formed. In this case, the thickness of the copper films 306 and 307 of a lower layer and the upper layer and a silver film 308 is adjusted so that the copper alloy film 309 which consists of Ag Cu-0.1% of the weight may be formed.
[0068] Next, as shown in drawing 6 (c), it continues on the embedding wiring 311 and an interlayer insulation film 302 on the whole surface, and the silicon nitride film 312 which prevents the diffusion to the upper part of Cu which constitutes the embedding wiring 311 is deposited.

[0069] Since the field made to react by heat treatment is restricted to the upper copper film 307 and the silver film 308 deposited alternatively according to the 3rd operation gestalt, the process which removes the film deposited on the interlayer insulation film 302 by the CMP method becomes easy.
[0070] In addition, in the 3rd operation gestalt, although the silver film 308 was alternatively deposited on the upper copper film 307, it replaces with this, and after covering the whole surface and depositing a silver film 308, heat treatment may be performed, the copper alloy film 309 may be formed, and the silver film 308 which remains may be removed by the CMP method after that.
[0071] (4th operation gestalt) Copper alloy wiring in the semiconductor device concerning the 4th operation gestalt of this invention and its manufacture approach are explained hereafter, referring to drawing 7 (a) - (c).
[0072] First, after forming a contact hole and the concave slot for wiring in the interlayer insulation film 402 deposited on the semi-conductor substrate 401 like the 3rd operation gestalt, on the interlayer insulation film 402 including a contact hole and the concave slot for wiring, the whole surface is covered and the TiN/Ti film 405 is deposited. After depositing the lower layer copper film 406 on the TiN/Ti film 405 by the spatter, with next, a CVD method or plating As the upper copper film 407 is deposited on the lower layer copper film 406, and the CMP method is performed after that as opposed to the copper films 406 and 407 of the TiN/Ti film 405, a lower layer, and the upper layer and it is shown in drawing 7 (a) The copper films 406 and 407 of the TiN/Ti film 405 exposed on an interlayer insulation film 402, a lower layer, and the upper layer are removed.
[0073] Next, as shown in drawing 7 (b), on the upper copper film 407 and an interlayer insulation film 402, the whole surface is covered and the alumina film 408 is deposited.
[0074] Next, aluminum 2O3 which heat-treats and constitutes the alumina film 408 As the copper films 406 and 407 of a lower layer and the upper layer are diffused and it is shown in drawing 7 (c), it is Cu-aluminum 2O3. While forming the becoming copper alloy film 409, the contact 410 and the embedding wiring 411 which consist of this copper alloy film 409 are formed.
[0075] Since the alumina film 408 can be used as an interlayer insulation film while not removing, since the alumina film 408 has insulation according to the 4th operation gestalt, reduction of a routing counter can be aimed at.
[0076] in addition, the 1- in the 4th operation gestalt, although the pure copper was used as copper films 107, 207, 307, and 407, it may replace with this and the copper alloy with which it comes to contain other metals in Cu may be used.
[0077] Moreover, the TiN/Ti film 105, 205, 305, and 405 or copper films 107, 207, 307, and 407 may be deposited only on the interior of contact holes 103, 203, and 303 and the concave slots 104, 204, and 304 for wiring with a selection CVD method, and other diffusion prevention film, for example, Ta film, TaN film, or WN film etc. may be used instead of the TiN/Ti film 105, 205, 305, and 405.
[0078] Moreover, if the embedding inside contact holes 103, 203, and 303 and the concave slots 104, 204, and 304 for wiring is possible, copper films 107, 207, and 307 may be formed by other approaches, such as the spatter + reflow method or the ion plating method.
[0079] Furthermore, in case the upper copper films 207, 307, and 407 are deposited, when you do not need the copper film of a substrate, you may omit the lower layer copper films 206, 306, and 406.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] (a) - (c) is the sectional view showing each process of the manufacture approach of the semiconductor device concerning the 1st operation gestalt.
[Drawing 2] (a) and (b) are the sectional views showing each process of the manufacture approach of the semiconductor device concerning the 1st operation gestalt.
[Drawing 3] (a) - (c) is the sectional view showing each process of the manufacture approach of the semiconductor device concerning the 2nd operation gestalt.
[Drawing 4] (a) - (c) is the sectional view showing each process of the manufacture approach of the semiconductor device concerning the 2nd operation gestalt.
[Drawing 5] (a) - (d) is the sectional view showing each process of the manufacture approach of the semiconductor device concerning the 3rd operation gestalt.
[Drawing 6] (a) - (c) is the sectional view showing each process of the manufacture approach of the semiconductor device concerning the 3rd operation gestalt.
[Drawing 7] (a) - (c) is the sectional view showing each process of the manufacture approach of the semiconductor device concerning the 4th operation gestalt.
[Drawing 8] It is the property Fig. in which reaching in the tension strength of various kinds of copper alloys, and showing conductivity.
[Description of Notations]
101 Semi-conductor Substrate
102 Interlayer Insulation Film
103 Contact Hole
104 Concave Slot for Wiring
105 TiN/Ti Film
106 Copper Alloy Film
107 Copper Film
108 Copper Alloy Film
109 Contact
110 Embedding Wiring
111 Silicon Nitride Film
201 Semi-conductor Substrate
202 Interlayer Insulation Film
203 Contact Hole
204 Concave Slot for Wiring
205 TiN/Ti Film
206 Lower Layer Copper Film
207 The Upper Copper Film
208 Niobium Film
209 Copper Alloy Film

210 Contact
211 Embedding Wiring
212 Silicon Nitride Film
301 Semi-conductor Substrate
302 Interlayer Insulation Film
303 Contact Hole
304 Concave Slot for Wiring
305 TiN/Ti Film
306 Lower Layer Copper Film
307 The Upper Copper Film
308 Silver Film
309 Copper Alloy Film
310 Contact
311 Embedding Wiring
312 Silicon Nitride Film
401 Semi-conductor Substrate
402 Interlayer Insulation Film
405 TiN/Ti Film
406 Lower Layer Copper Film
407 The Upper Copper Film
408 Alumina Film

[Translation done.]

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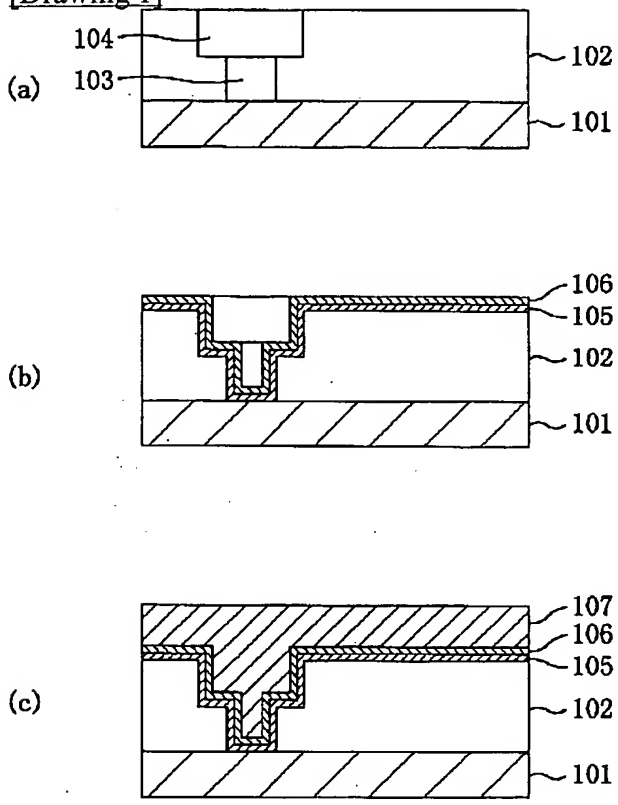
3.In the drawings, any words are not translated.

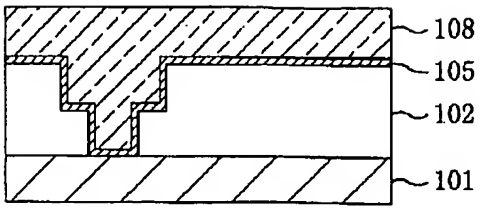
DRAWINGS

[Drawing 1]



[Drawing 2]

(a)



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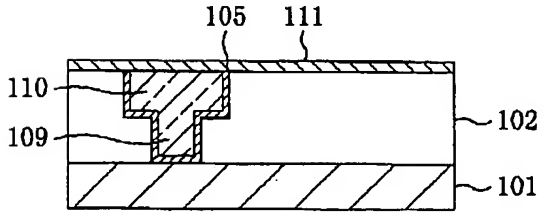
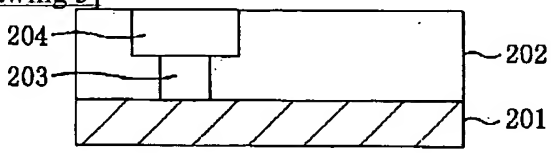


[Drawing 3]

(a)



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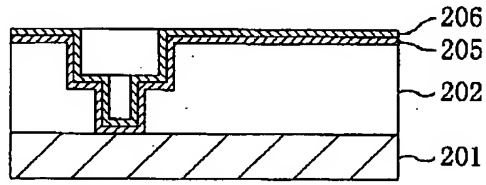

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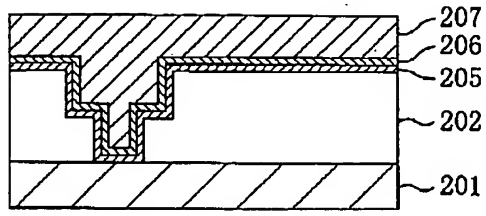
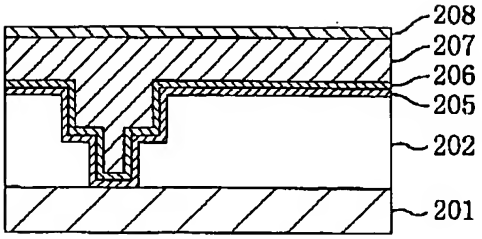


[Drawing 4]

(a)



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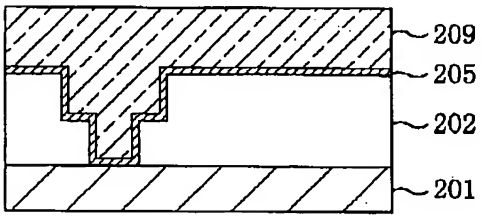

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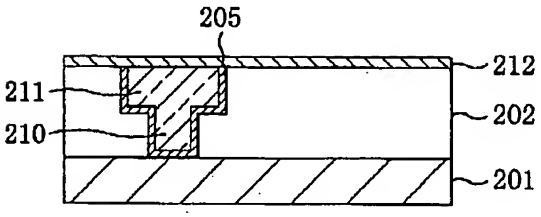
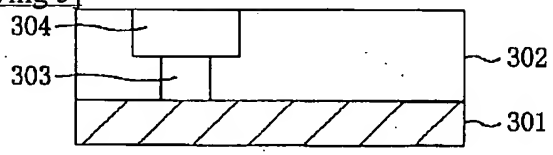


[Drawing 5]

(a)



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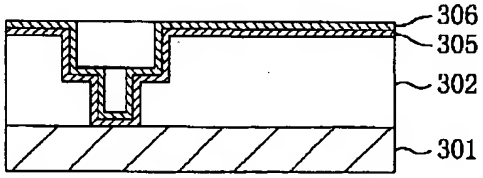

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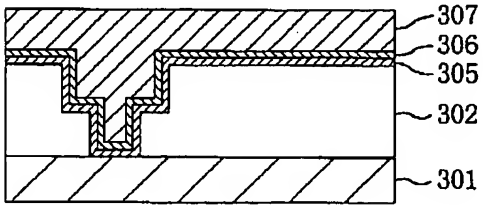
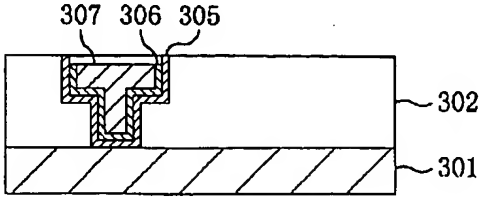
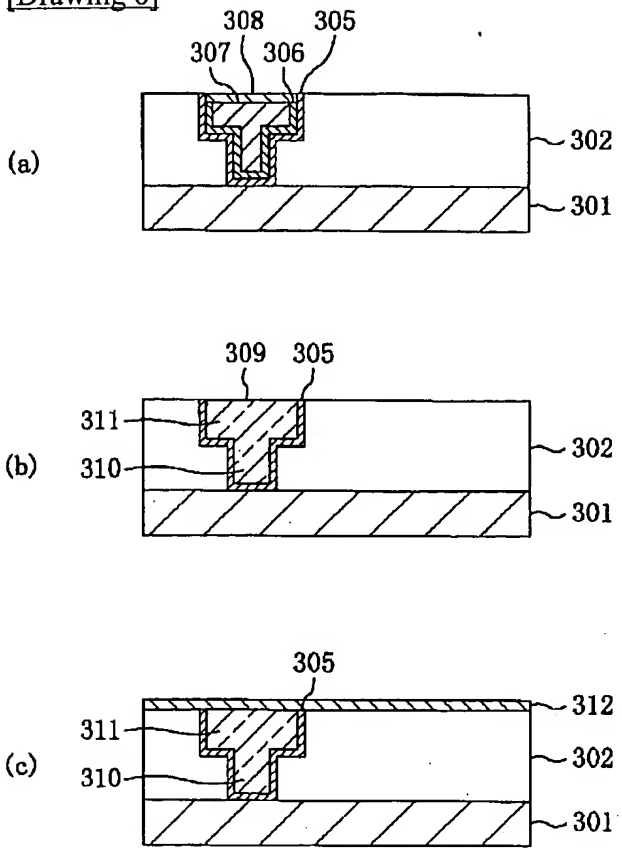


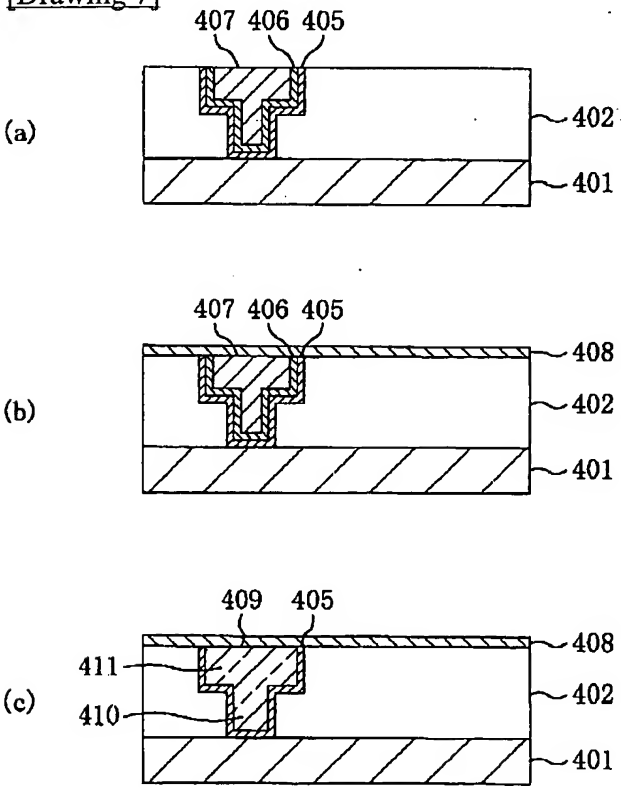
(d)



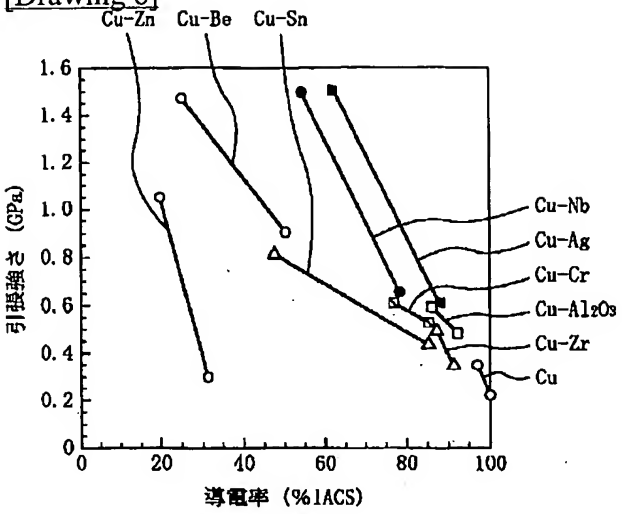
[Drawing 6]



[Drawing 7]



[Drawing 8]



[Translation done.]